



**YAREN**  
TECHNOLOGY

75N08  
Power MOSFET

## 80 Amps, 7.5 Volts N-CHANNEL POWER MOSFET

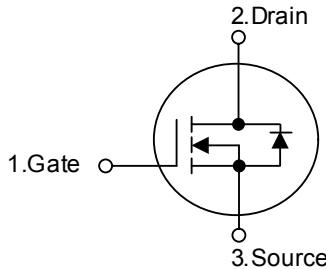
### ■ DESCRIPTION

This MOSFET process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced high-efficiency, high-frequency isolated DC-DC converters for Telecom and Computer applications. It is also intended for any applications with low gate drive requirements.

### ■ FEATURES

- TYPICAL  $R_{DS(on)}$  = 0.009Ω
- EXCEPTIONAL dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- LOW THRESHOLD DRIVE

### ■ SYMBOL



### ■ ABSOLUTE MAXIMUM RATINGS

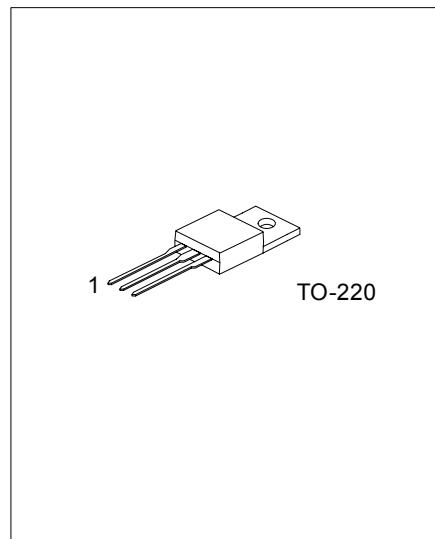
Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source Voltage ( $V_{GS} = 0$ )	75	V
$V_{DGR}$	Drain-gate Voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	75	V
$V_{GS}$	Gate-source Voltage	$\pm 20$	V
$I_D(\bullet)$	Drain Current (continuous) at $T_C = 25^\circ\text{C}$	80	A
$I_D$	Drain Current (continuous) at $T_C = 100^\circ\text{C}$	75	A
$I_{DM(\bullet\bullet)}$	Drain Current (pulsed)	320	A
$P_{tot}$	Total Dissipation at $T_C = 25^\circ\text{C}$	320	W
	Derating Factor	2	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	20	V/ns
$E_{AS}$ (2)	Single Pulse Avalanche Energy	680	mJ
$T_{stg}$	Storage Temperature	-55 to 175	°C
$T_j$	Max. Operating Junction Temperature		

(•) Current limited by package

(••) Pulse width limited by safe operating area.

(1)  $I_{sp} \leq 75\text{A}$ ,  $di/dt \leq 500\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_j \leq T_{JMAX}$ .

(2) Starting  $T_j = 25^\circ\text{C}$ ,  $I_D = 40\text{A}$ ,  $V_{DD} = 30\text{V}$



\*Pb-free plating product number: 75N08

## ■ THERMAL DATA

R <sub>thj-case</sub> R <sub>thj-amb</sub> T <sub>j</sub>	Thermal Resistance Junction-case Thermal Resistance Junction-ambient Maximum Lead Temperature For Soldering Purpose	Max Max Typ	0.5 62.5 300	°C/W °C/W °C
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## ■ ELECTRICAL CHARACTERISTICS T<sub>C</sub> = 25 °C unless otherwise specified

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source Breakdown Voltage	I <sub>D</sub> = 250 µA V <sub>GS</sub> = 0	75			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max Rating V <sub>DS</sub> = Max Rating T <sub>C</sub> = 125°C			25 25	µA µA
I <sub>GSS</sub>	Gate-body Leakage Current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 20 V			±100	nA

ON (\*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> I <sub>D</sub> = 250 µA	2		4	V
R <sub>DSS(on)</sub>	Static Drain-source On Resistance	V <sub>GS</sub> = 10 V I <sub>D</sub> = 40 A V <sub>GS</sub> = 5 V I <sub>D</sub> = 40 A		0.0075 0.0085	0.009 0.010	Ω Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub> (*)	Forward Transconductance	V <sub>DS</sub> = 20 V I <sub>D</sub> = 40		50		S
C <sub>iss</sub> C <sub>oss</sub> C <sub>rss</sub>	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V <sub>DS</sub> = 25V, f = 1 MHz, V <sub>GS</sub> = 0		4300 660 205		pF pF pF

## ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t <sub>d(on)</sub> t <sub>r</sub>	Turn-on Delay Time Rise Time	V <sub>DD</sub> = 40 V I <sub>D</sub> = 40 A R <sub>G</sub> = 4.7 Ω V <sub>GS</sub> = 4.5 V (Resistive Load, Figure 3)		35 150		ns ns
Q <sub>g</sub> Q <sub>gs</sub> Q <sub>gd</sub>	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V <sub>DD</sub> = 60V I <sub>D</sub> = 80 A V <sub>GS</sub> = 5V		75 18 31	90	nC nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t <sub>d(off)</sub> t <sub>f</sub>	Turn-off Delay Time Fall Time	V <sub>DD</sub> = 40 V I <sub>D</sub> = 40 A R <sub>G</sub> = 4.7Ω, V <sub>GS</sub> = 4.5 V (Resistive Load, Figure 3)		110 60		ns ns

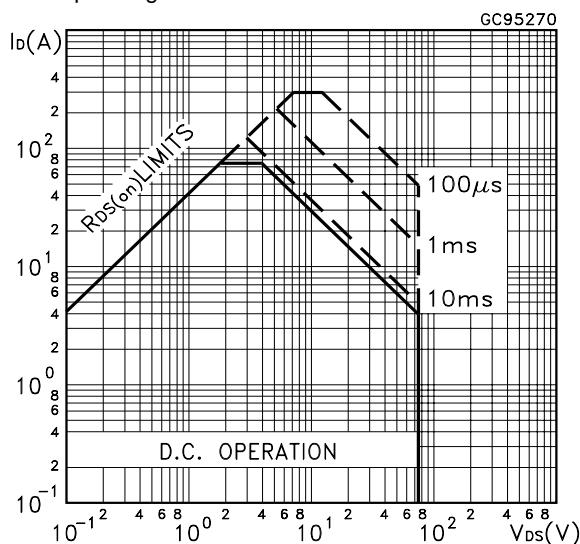
SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I <sub>SD</sub> I <sub>SDM</sub> (*)	Source-drain Current Source-drain Current (pulsed)				80 320	A A
V <sub>SD</sub> (*)	Forward On Voltage	I <sub>SD</sub> = 80 A V <sub>GS</sub> = 0			1.4	V
t <sub>rr</sub> Q <sub>rr</sub> I <sub>RRM</sub>	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I <sub>SD</sub> = 80 Adi/dt = 100A/µs V <sub>DD</sub> = 20 V T <sub>j</sub> = 150°C (see test circuit, Figure 5)		100 380 7.5		ns nC A

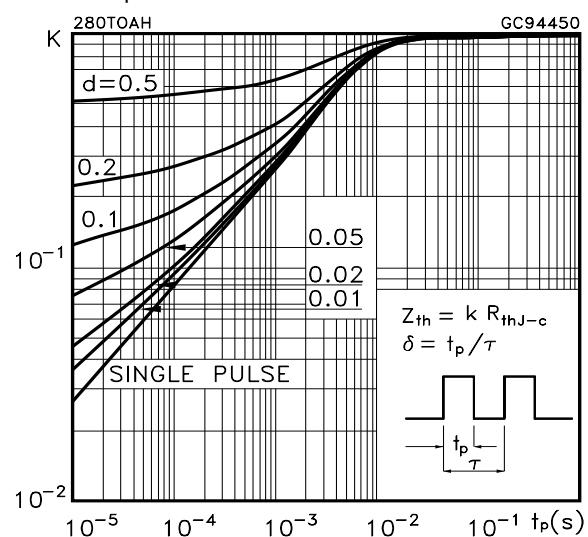
(\*)Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.

(•)Pulse width limited by safe operating area.

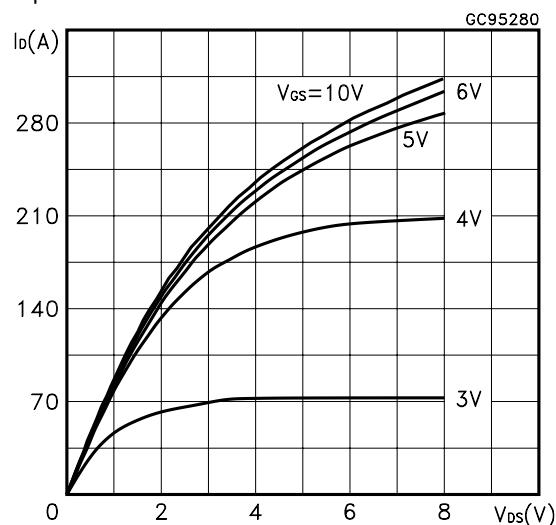
Safe Operating Area



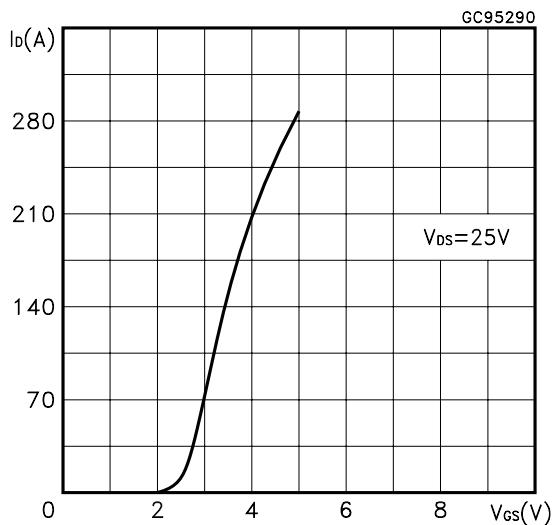
Thermal Impedance



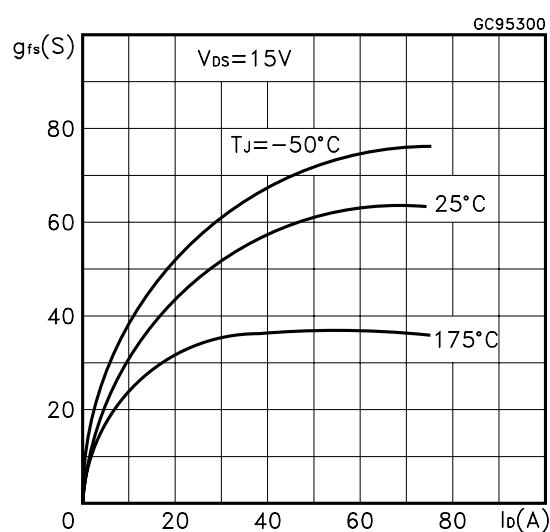
Output Characteristics



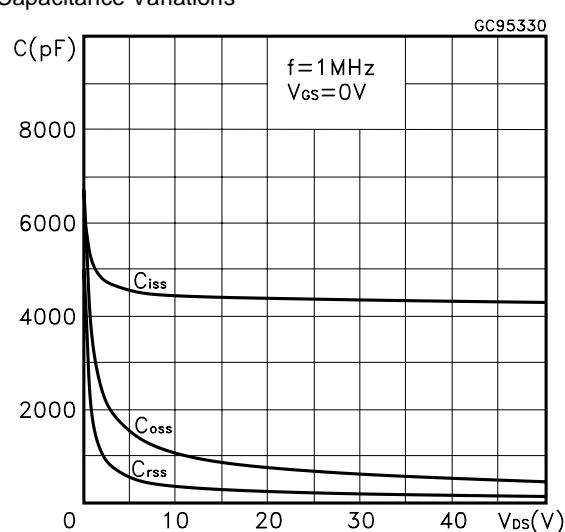
Transfer Characteristics



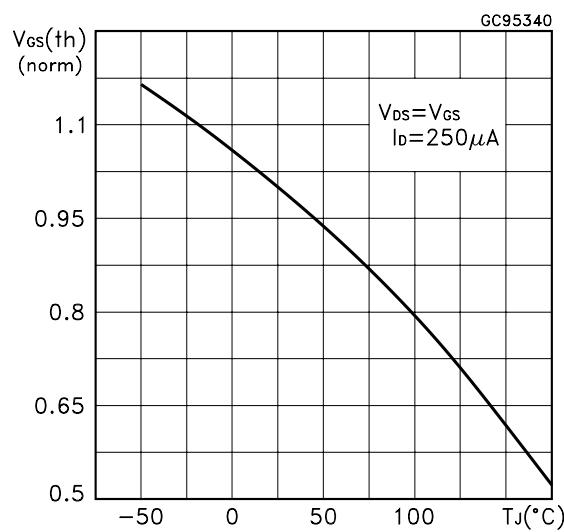
Transconductance



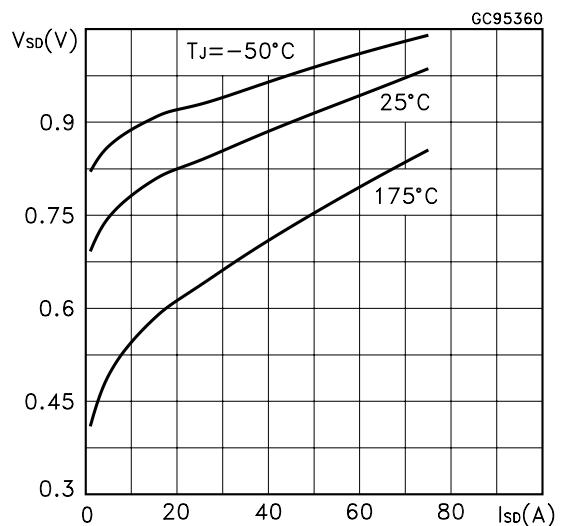
Capacitance Variations



Normalized Gate Threshold Voltage vs Temperature



Source-drain Diode Forward Characteristics



Normalized Breakdown Voltage vs Temperature.

