# 5.5 Amps, 650 Volts
N-CHANNEL MOSFET

■ **DESCRIPTION**

The YR6N60 is a high voltage MOSFET and is designed to have better characteristics, such as fast switching time, low gate charge, low on-state resistance and have a high rugged avalanche characteristics. This power MOSFET is usually used at high speed switching applications in switching power supplies and adaptors.

■ **FEATURES**

* $R_{DS(ON)}$ = 2.5Ω @V_{GS} = 10V
* Ultra low gate charge (typical 20 nC)
* Low reverse transfer Capacitance (C_{RSS} = typical 10pF)
* Fast switching capability
* Avalanche energy tested
* Improved dv/dt capability, high ruggedness

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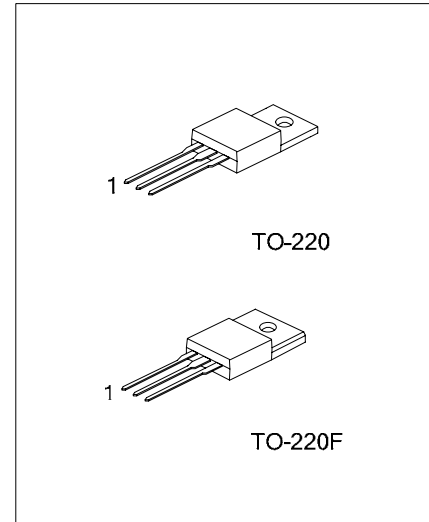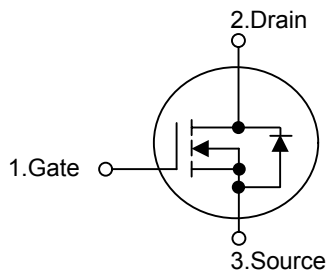
*Pb-free plating product number: 6N60

■ **SYMBOL**

2.Drain

1.Gate

3.Source

6N65

■ **ABSOLUTE MAXIMUM RATINGS** (T$_C$ = 25, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage	6N60	V$_{DSS}$	600	V
	6N65		650	V
Gate-Source Voltage		V$_{GSS}$	±20	V
Avalanche Current (Note 1)		I$_{AR}$	5.5	A
Continuous Drain Current	T$_C$ = 25°C	I$_D$	5.5	A
	T$_C$ = 100°C		3.4	A
Pulsed Drain Current (Note 1)		I$_{DM}$	24.8	A
Avalanche Energy	Single Pulsed (Note 2)	E$_{AS}$	440	mJ
	Repetitive (Note 1)	E$_{AR}$	13	mJ
Power Dissipation		P$_D$	62.5	W
Junction Temperature		T$_J$	+150	
Operating Temperature		T$_{OPR}$	-55 ~ +150	
Storage Temperature		T$_{STG}$	-55 ~ +150	

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.
Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ **THERMAL DATA**

PARAMETER	SYMBOL	RATING	UNIT
Junction-to-Ambient	θ$_{JA}$	62	°C/W
Junction-to-Case	θ$_{JC}$	2	°C/W

■ **ELECTRICAL CHARACTERISTICS** (T$_J$=25, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage	6N60	BV$_{DSS}$	V$_{GS}$ = 0V, I$_D$ = 250µA	600			V
	6N65			650			V
Drain-Source Leakage Current		I$_{DSS}$	V$_{DS}$ = 600V, V$_{GS}$ = 0V			10	µA
Gate- Source Leakage Current	Forward	I$_{GSS}$	V$_{GS}$ = 20V, V$_{DS}$ = 0V			100	nA
	Reverse		V$_{GS}$ = -20V, V$_{DS}$ = 0V			-100	nA
Breakdown Voltage Temperature Coefficient		BV$_{DSS}$/ T$_J$	I$_D$ = 250 µA, Referenced to 25°C		0.53		V/
ON CHARACTERISTICS							
Gate Threshold Voltage		V$_{GS(TH)}$	V$_{DS}$ = V$_{GS}$, I$_D$ = 250µA	2.0		4.0	V
Static Drain-Source On-State Resistance		R$_{DS(ON)}$	V$_{GS}$ = 10V, I$_D$ = 2.75A		2.1	2.5	Ω
DYNAMIC CHARACTERISTICS							
Input Capacitance		C$_{ISS}$			770	1000	pF
Output Capacitance		C$_{OSS}$	V$_{DS}$=25V, V$_{GS}$=0V, f=1.0 MHz		95	120	pF
Reverse Transfer Capacitance		C$_{RSS}$			10	13	pF
SWITCHING CHARACTERISTICS							
Turn-On Delay Time		t$_{D(ON)}$			20	50	ns
Turn-On Rise Time		t$_R$	V$_{DD}$=300V, I$_D$ =5.5A, R$_G$ =25Ω		70	150	ns
Turn-Off Delay Time		t$_{D(OFF)}$	(Note 4, 5)		40	90	ns
Turn-Off Fall Time		t$_F$			45	100	ns
Total Gate Charge		Q$_G$	V$_{DS}$=480V, I$_D$=5.5A, V$_{GS}$=10 V		20	25	nC
Gate-Source Charge		Q$_{GS}$	(Note 4, 5)		4.9		nC
Gate-Drain Charge		Q$_{GD}$			9.4		nC

■ **ELECTRICAL CHARACTERISTICS**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
Drain-Source Diode Forward Voltage	V_{SD}	V_{GS} = 0 V, I_S = 5.5 A			1.4	V
Maximum Continuous Drain-Source Diode Forward Current	I_S				6.0	A
Maximum Pulsed Drain-Source Diode Forward Current	I_{SM}				24.8	A
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, I_S = 5.5 A,		290		ns
Reverse Recovery Charge	Q_{RR}	dI_F/dt = 100 A/μs (Note 4)		2.35		μC

Notes: 1. Repetitive Rating : Pulse width limited by T_J

2. L = 16.8mH, I_{AS} = 5.5A, V_{DD} = 90V, R_G = 25 Ω, Starting T_J = 25°C

3. I_{SD} ≤ 5.5A, di/dt ≤200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C

4. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%

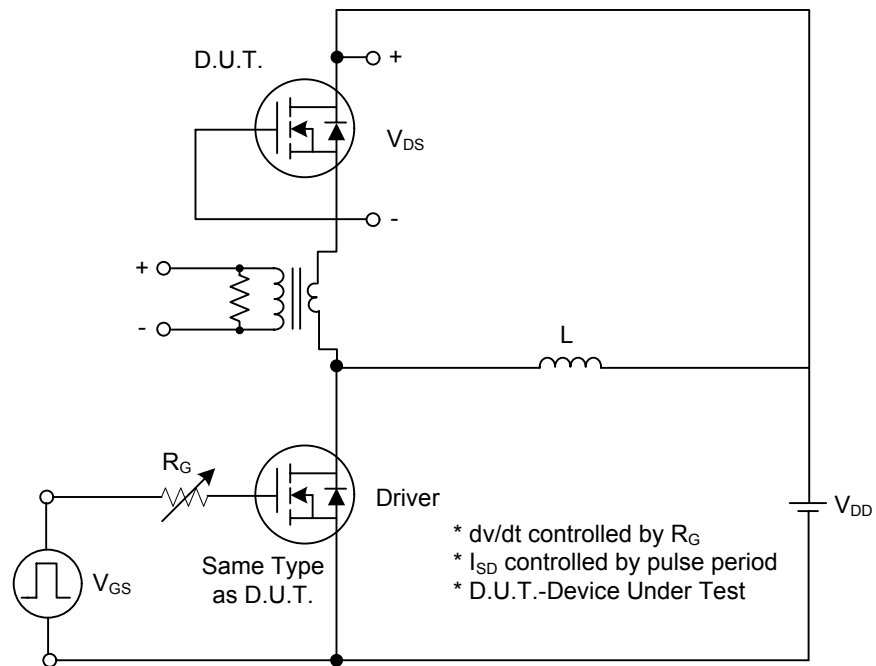5. Essentially independent of operating temperature

■ **TEST CIRCUITS AND WAVEFORMS**
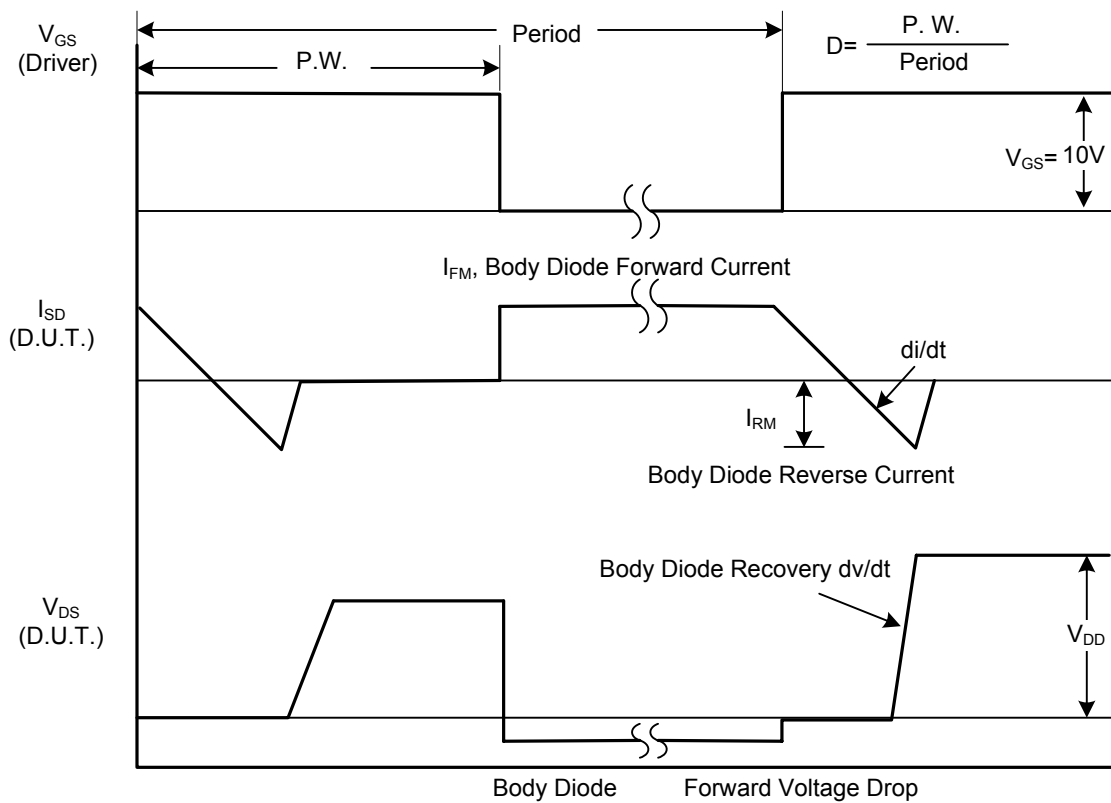

Fig. 1A Peak Diode Recovery dv/dt Test Circuit

* dv/dt controlled by R_G
* I_{SD} controlled by pulse period
* D.U.T.-Device Under Test

Fig. 1B Peak Diode Recovery dv/dt Waveforms

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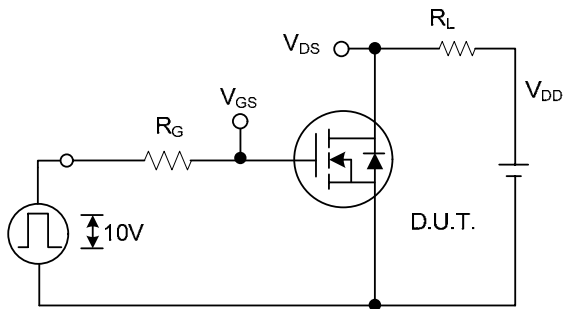■ **TEST CIRCUITS AND WAVEFORMS (Cont.)**
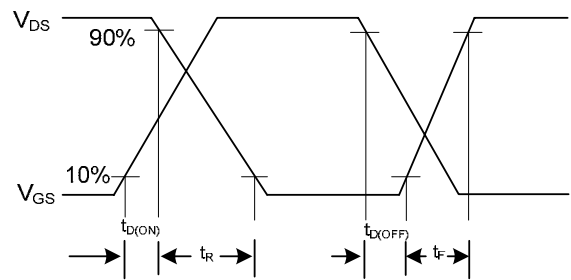

Fig. 2A Switching Test Circuit
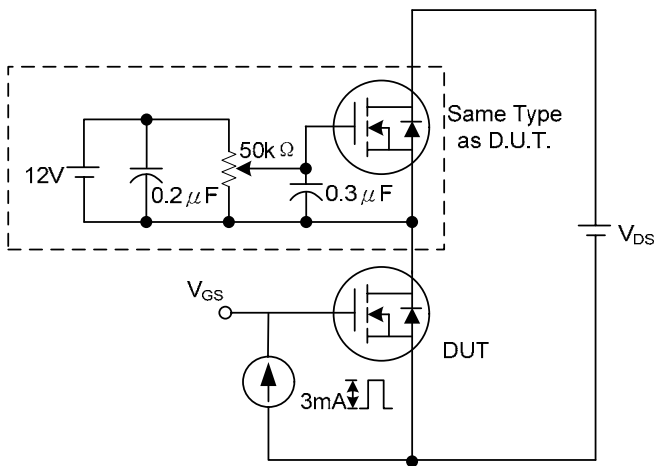

Fig. 2B Switching Waveforms
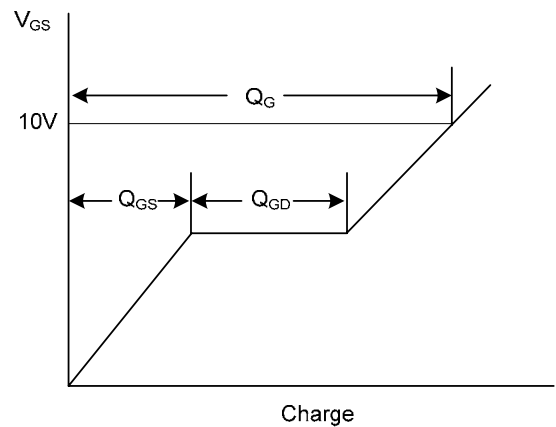

Fig. 3A Gate Charge Test Circuit

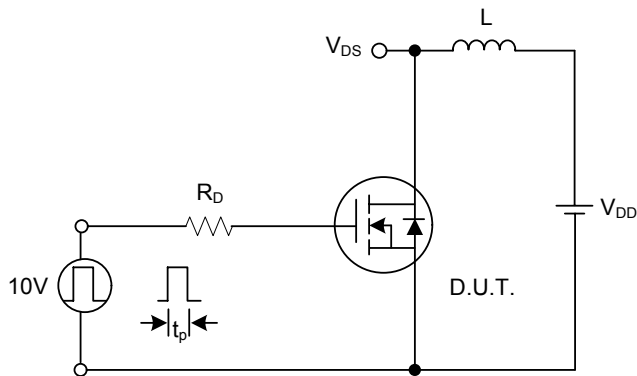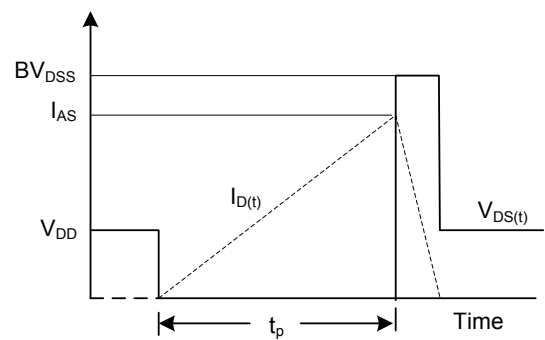**Fig. 3B Gate Charge Waveform**

Fig. 4A Unclamped Inductive Switching Test Circuit

Fig. 4B Unclamped Inductive Switching Waveforms