YAREN
TECHNOLOGY

8 4 Amps,   6 0 Volts
N-CHANNEL POWER MOSFET
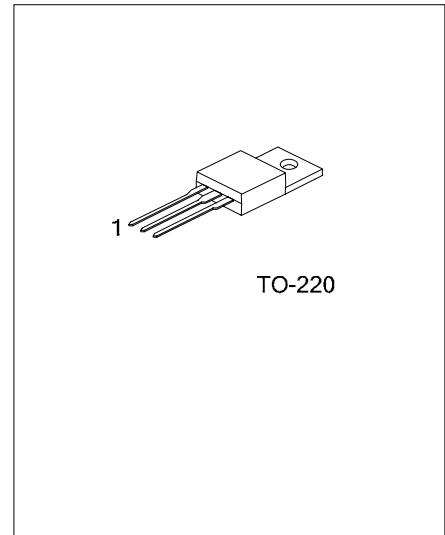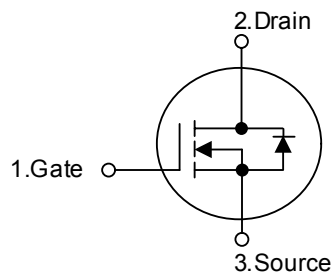
■ DESCRIPTION

The YR 1010E is three-terminal silicon device with current conduction capability of about 84A, fast switching speed. Low on-state resistance, breakdown voltage rating of 60V, and max threshold voltages of 4 volt.

It is mainly suitable electronic ballast, and low power switching mode power appliances.

■ FEATURES

* $R_{DS(ON)}$ = 12mΩ@V_{GS} = 10 V
* Ultra low gate charge (typical 200 nC)
* Low reverse transfer Capacitance (C_{RSS} = typical 160 pF)
* Fast switching capability
* 100% avalanche energy specified
* Improved dv/dt capability
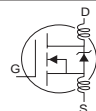

TO-220

*Pb-free plating product number: YR1010E

■ SYMBOL

2.Drain

1.Gate

3.Source

Absolute Maximum Ratings

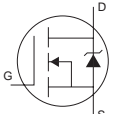|	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	84⑦	
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	59	A
I_{DM}	Pulsed Drain Current ①	330	
P_D @T_C = 25°C	Power Dissipation	200	W
	Linear Derating Factor	1.4	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
I_{AR}	Avalanche Current①	50	A
E_{AR}	Repetitive Avalanche Energy①	17	mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.0	V/ns
T_J	Operating Junction and	-55 to + 175	
T_{STG}	Storage Temperature Range		°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 srew	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	0.75	
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	——	°C/W
$R_{\theta JA}$	Junction-to-Ambient	——	62	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	60	——	——	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.064	——	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	——	12	mΩ	V_{GS} = 10V, I_D = 50A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	——	4.0	V	V_{DS} = V_{GS}, I_D = 250µA
g_{fs}	Forward Transconductance	69	——	——	S	V_{DS} = 25V, I_D = 50A④
I_{DSS}	Drain-to-Source Leakage Current	——	——	25	µA	V_{DS} = 60V, V_{GS} = 0V
		——	——	250		V_{DS} = 48V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	——	——	-100		V_{GS} = -20V
Q_g	Total Gate Charge	——	——	130	nC	I_D = 50A
Q_{gs}	Gate-to-Source Charge	——	——	28		V_{DS} = 48V
Q_{gd}	Gate-to-Drain ("Miller") Charge	——	——	44		V_{GS} = 10V, See Fig. 6 and 13
$t_{d(on)}$	Turn-On Delay Time	——	12	——	ns	V_{DD} = 30V
t_r	Rise Time	——	78	——		I_D = 50A
$t_{d(off)}$	Turn-Off Delay Time	——	48	——		R_G = 3.6Ω
t_f	Fall Time	——	53	——		V_{GS} = 10V, See Fig. 10 ④
L_D	Internal Drain Inductance	——	4.2	——	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	——	8.5	——		
C_{iss}	Input Capacitance	——	3210	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	690	——		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	——	140	——		f = 1.0MHz, See Fig. 5
E_{AS}	Single Pulse Avalanche Energy②	——	1280⑤	320⑥	mJ	I_{AS} = 50A, L = 260µH

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	84⑦	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode)①	——	——	330		
V_{SD}	Diode Forward Voltage	——	——	1.3	V	T_J = 25°C, I_S = 50A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	——	73	110	ns	T_J = 25°C, I_F = 50A
Q_{rr}	Reverse Recovery Charge	——	220	330	nC	di/dt = 100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② Starting T_J = 25°C, L = 260µH
 R_G = 25Ω, I_{AS} = 50A, V_{GS} =10V (See Figure 12)

③ $I_{SD} \le$ 50A, di/dt $\le$ 230A/µs, $V_{DD} \le V_{(BR)DSS}$,
 $T_J \le$ 175°C

④ Pulse width $\le$ 400µs; duty cycle $\le$ 2%.

⑤ This is a typical value at device destruction and represents operation outside rated limits.

⑥ This is a calculated value limited to T_J = 175°C .

⑦ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A.
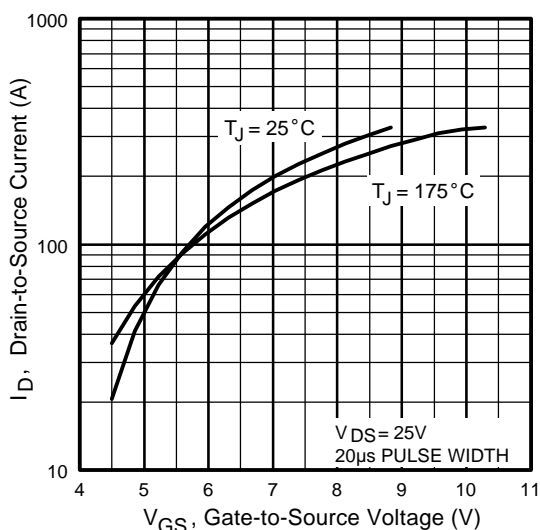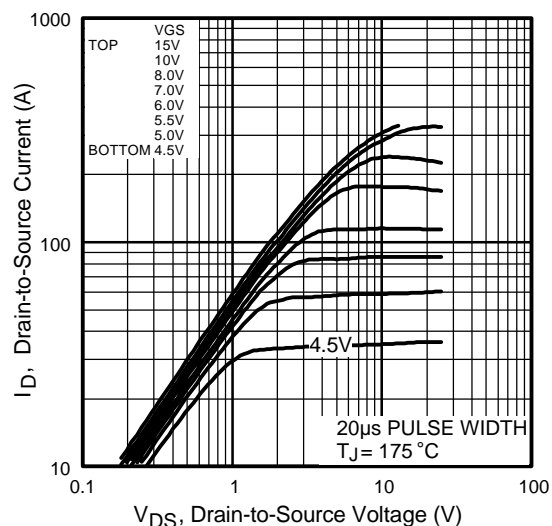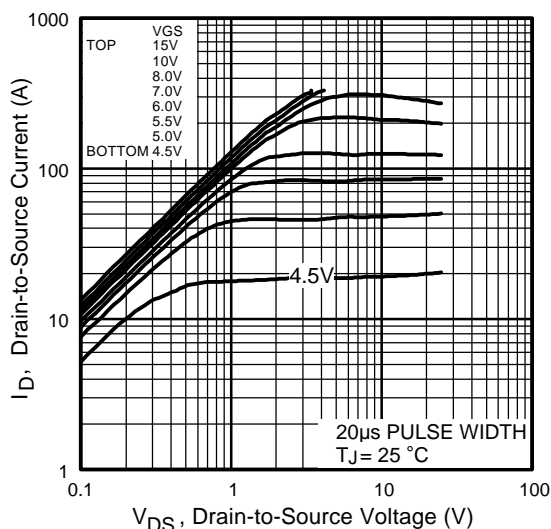

Fig 3. Typical Transfer Characteristics

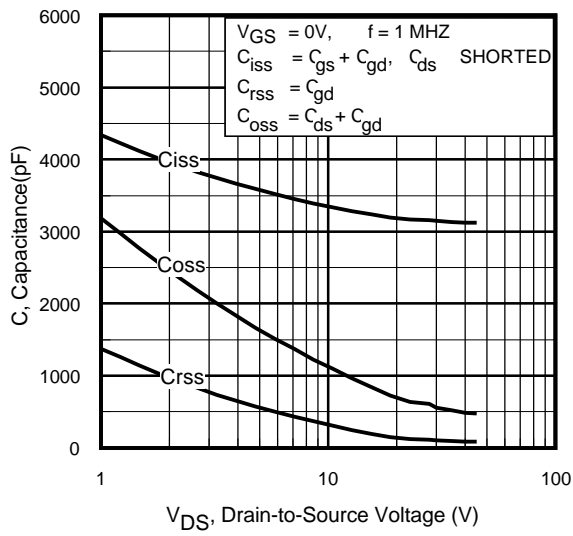**Fig 4.** Normalized On-Resistance Vs. Temperature

Fig 5. Typical Capacitance Vs.
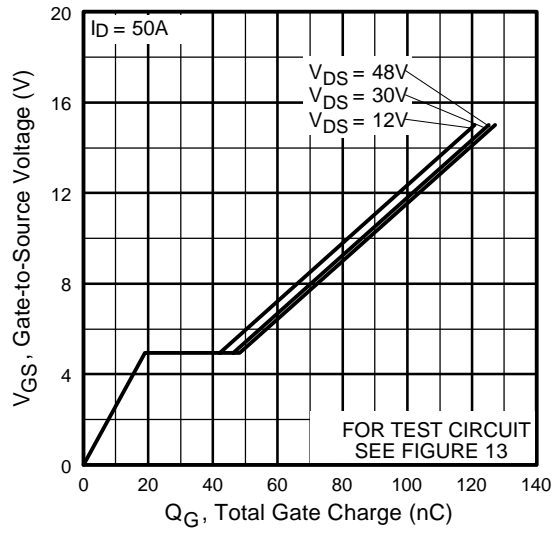Drain-to-Source Voltage
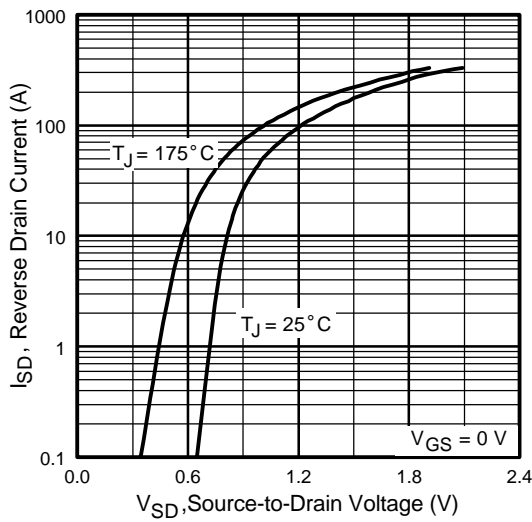

Fig 6. Typical Gate Charge Vs.
Gate-to-Source Voltage
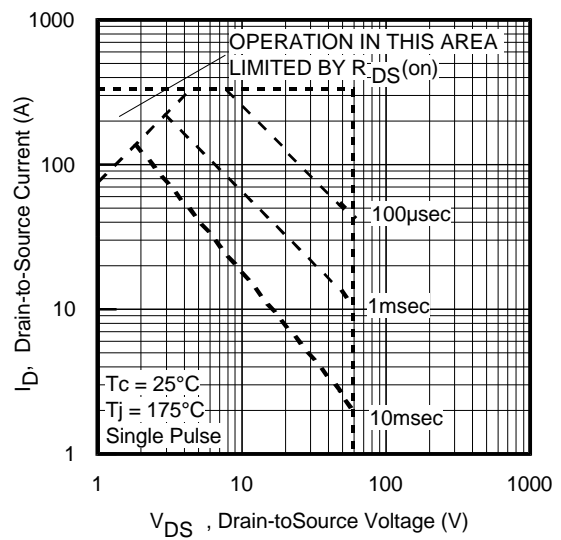

Fig 7. Typical Source-Drain Diode
Forward Voltage

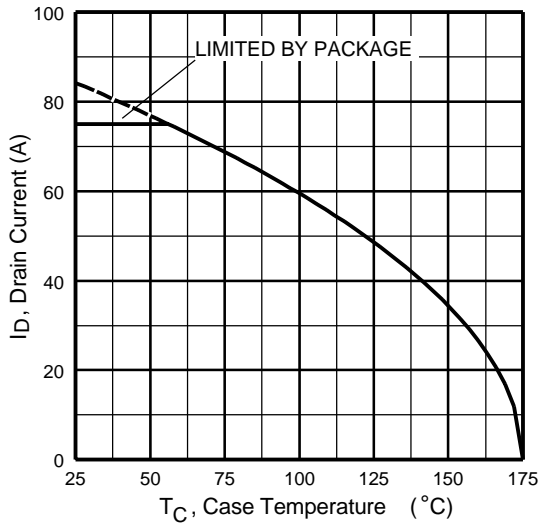

Fig 8. Maximum Safe Operating Area

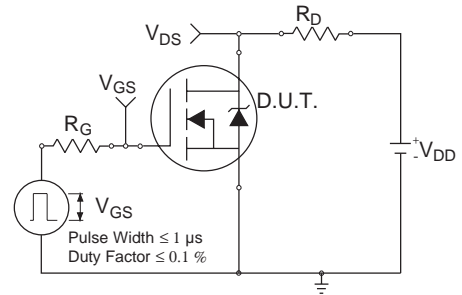**Fig 9.** Maximum Drain Current Vs. Case Temperature

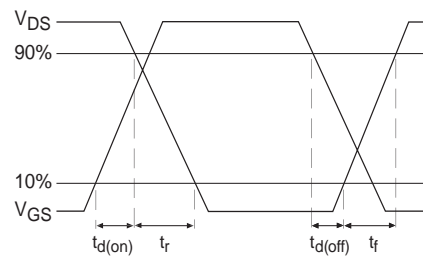**Fig 10a.** Switching Time Test Circuit

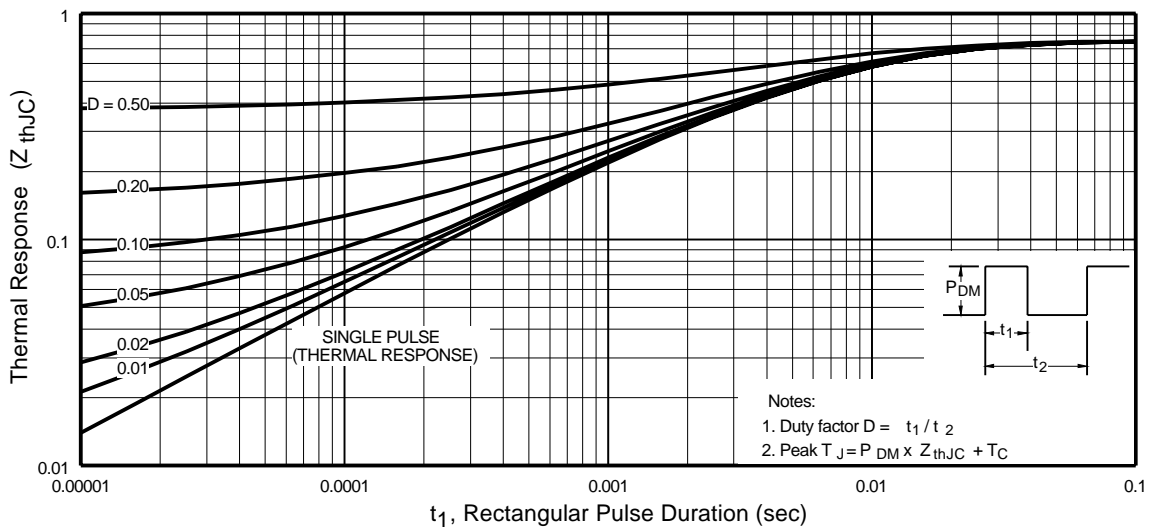**Fig 10b.** Switching Time Waveforms

Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case
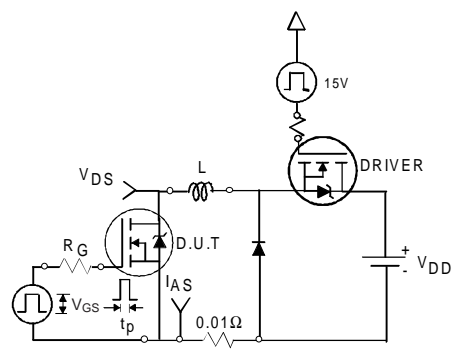
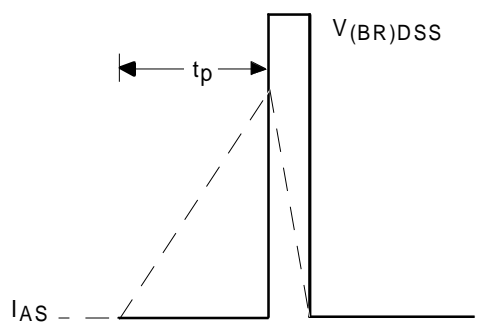**Fig 12a.** Unclamped Inductive Test Circuit

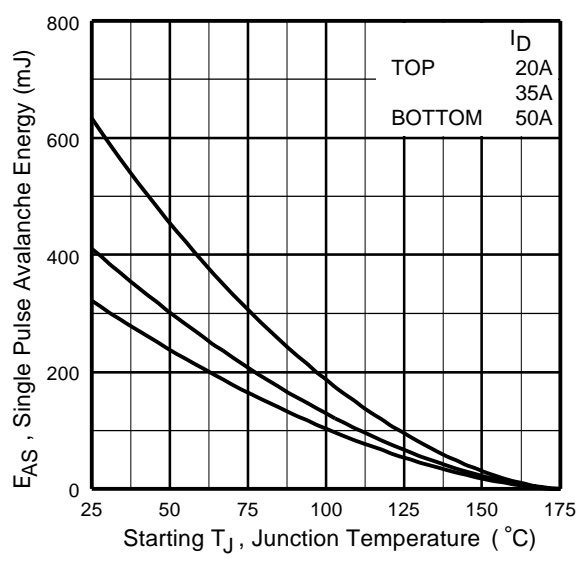**Fig 12b.** Unclamped Inductive Waveforms

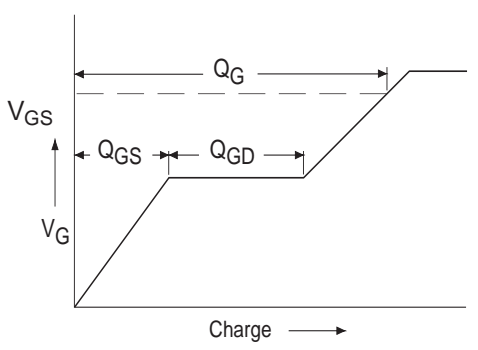**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current
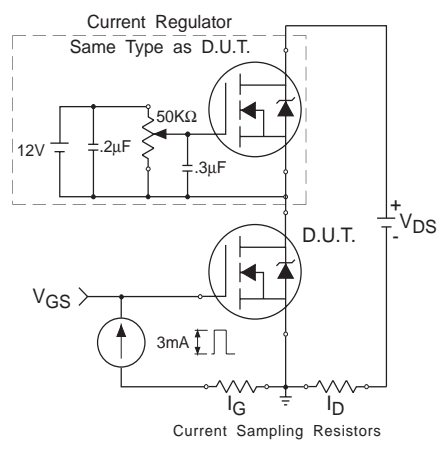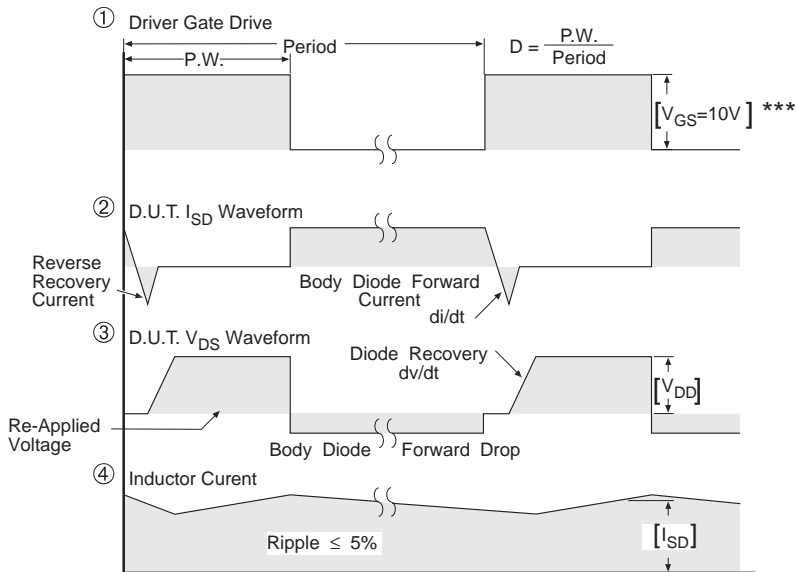
Fig 13a. Basic Gate Charge Waveform

Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit

D.U.T*

③

Circuit Layout Considerations
- Low Stray Inductance
- Ground Plane
- Low Leakage Inductance Current Transformer

②

④

①

R_G

- dv/dt controlled by R_G
- I_{SD} controlled by Duty Factor "D"
- D.U.T. - Device Under Test

V_{GS}

V_{DD}

* Reverse Polarity of D.U.T for P-Channel

① Driver Gate Drive

P.W.

Period

$D = \dfrac{P.W.}{Period}$

$\left[V_{GS} = 10V \right]$ ***

② D.U.T. I_{SD} Waveform

Reverse Recovery Current

Body Diode Forward Current

di/dt

③ D.U.T. V_{DS} Waveform

Diode Recovery dv/dt

$\left[V_{DD} \right]$

Re-Applied Voltage

Body Diode Forward Drop

④ Inductor Curent

Ripple ≤ 5%

$\left[I_{SD} \right]$

*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

For N-channel HEXFET®