



25Amps, 400 Volts N-CHANNEL MOSFET

■ DESCRIPTION

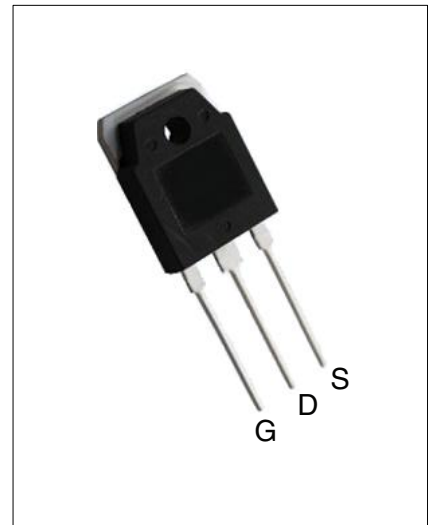
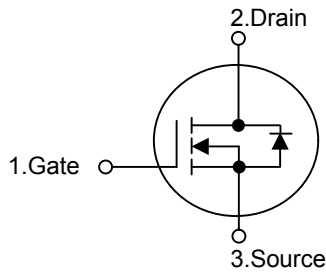
The YRIRF360 are N-Channel enhancement mode power field effect transistors (MOSFET) which are produced using YR's proprietary, planar stripe, DMOS technology.

These devices are suited for high efficiency switch mode power supply. To minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode the advanced technology has been especially tailored.

■ FEATURES

- * $R_{DS(ON)} = 0.20\Omega$ @ $V_{GS} = 10V$
- * Ultra low gate charge (typical 42 nC)
- * Low reverse transfer capacitance ($C_{RSS} =$ typical 400 pF)
- * Fast switching capability
- * Avalanche energy specified
- * Improved dv/dt capability, high ruggedness

■ SYMBOL



*Pb-free plating product number:IRF360

■ ABSOLUTE MAXIMUM RATINGS ($T_C = 25$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage	IRF360	V_{DSS}	400	V
Gate-Source Voltage		V_{GSS}	± 20	V
Avalanche Current (Note 1)		I_{AR}	25	A
Continuous Drain Current		I_D	25	A
Pulsed Drain Current (Note 1)		I_{DM}	100	A
Avalanche Energy	Single Pulsed (Note 2)	E_{AS}	980	mJ
	Repetitive (Note 1)	E_{AR}	30	mJ
Peak Diode Recovery dv/dt (Note 3)		dv/dt	4	V/ns
Junction Temperature		T_J	+150	
Operating Temperature		T_{OPR}	-55 ~ +150	
Storage Temperature		T_{STG}	-55 ~ +150	

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ ELECTRICAL CHARACTERISTICS ($T_C = 25$, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
OFF CHARACTERISTICS								
Drain-Source Breakdown Voltage	IRF360	BV_{DSS}	$V_{GS} = 0\text{ V}, I_D = 1.0\text{mA}$	400			V	
Drain-Source Leakage Current		I_{DSS}	$V_{DS} = 320\text{ V}, V_{GS} = 0\text{ V}$			10	μA	
Gate-Source Leakage Current		I_{GSS}	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$			± 100	nA	
Breakdown Voltage Temperature Coefficient		BV_{DSS}/T_J	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C		0.46		V/	
ON CHARACTERISTICS								
Gate Threshold Voltage		$V_{GS(TH)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0		4.0	V	
Static Drain-Source On-State Resistance		$R_{DS(ON)}$	$V_{GS} = 10\text{V}, I_D = 16\text{A}$			0.20	Ω	
DYNAMIC CHARACTERISTICS								
Input Capacitance		C_{ISS}	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{MHz}$		4200		pF	
Output Capacitance		C_{OSS}				900		pF
Reverse Transfer Capacitance		C_{RSS}				400		pF
SWITCHING CHARACTERISTICS								
Turn-On Delay Time		$t_{D(ON)}$	$V_{DD} = 200\text{V}, I_D = 25\text{A}, R_G = 25\Omega$ (Note 4, 5)			33	ns	
Turn-On Rise Time		t_R				140	ns	
Turn-Off Delay Time		$t_{D(OFF)}$				120	ns	
Turn-Off Fall Time		t_F				99	ns	
Total Gate Charge		Q_G	$V_{DS} = 400\text{V}, I_D = 25\text{A}, V_{GS} = 10\text{ V}$ (Note 4, 5)			210	nC	
Gate-Source Charge		Q_{GS}				28	nC	
Gate-Drain Charge		Q_{GD}				120	nC	
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS								
Drain-Source Diode Forward Voltage		V_{SD}	$V_{GS} = 0\text{ V}, I_S = 25\text{A}$			1.7	V	
Maximum Continuous Drain-Source Diode Forward Current		I_S				25	A	
Maximum Pulsed Drain-Source Diode Forward Current		I_{SM}				100	A	
Reverse Recovery Time		t_{RR}	$V_{GS} = 0\text{ V}, I_S = 25\text{A}$,			1000	ns	
Reverse Recovery Charge		Q_{RR}	$dI_F/dt = 100\text{ A}/\mu\text{s}$ (Note 4)			16	μC	

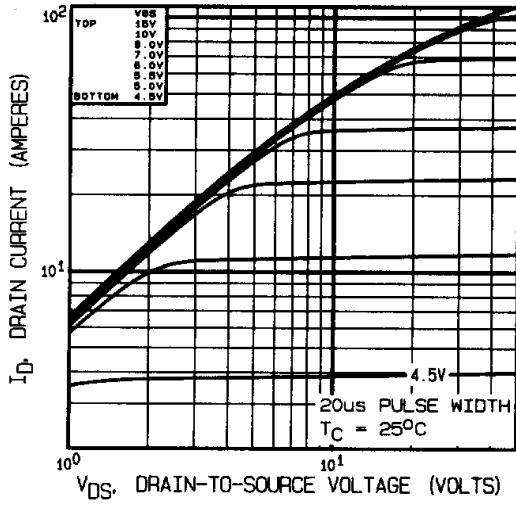


Fig 1. Typical Output Characteristics

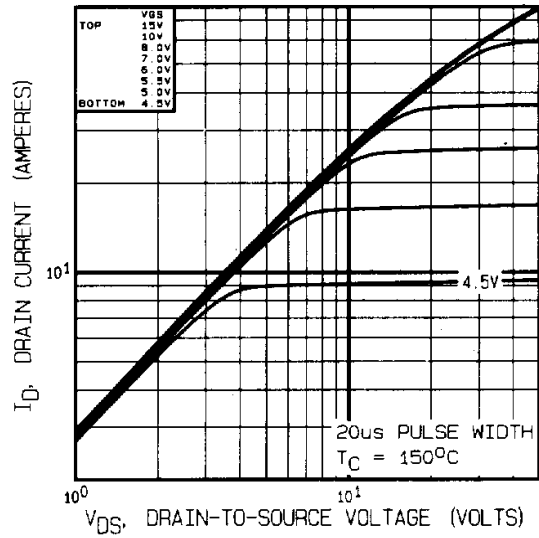


Fig 2. Typical Output Characteristics

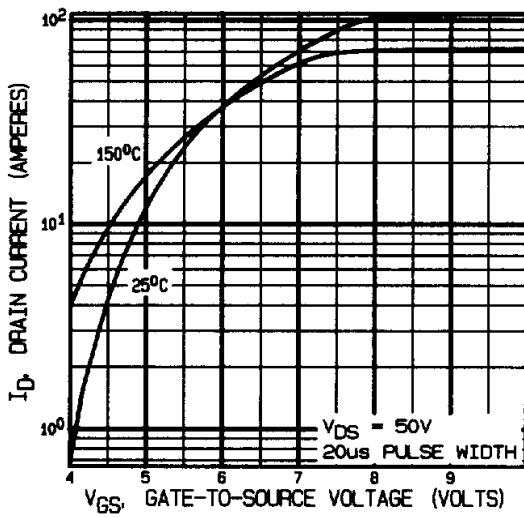


Fig 3. Typical Transfer Characteristics

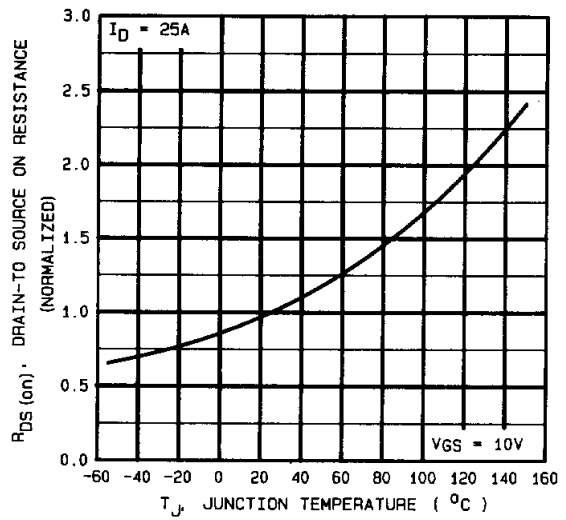


Fig 4. Normalized On-Resistance Vs. Temperature

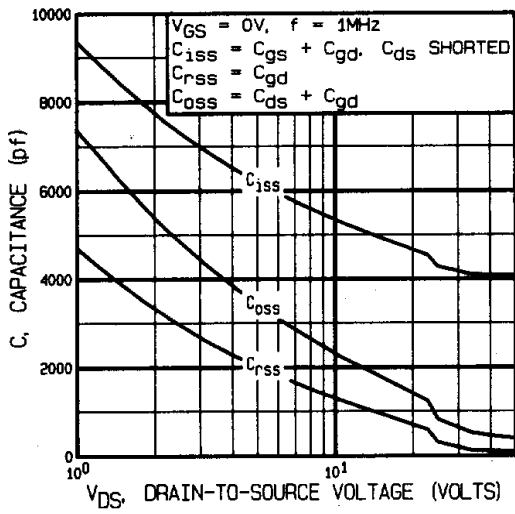


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

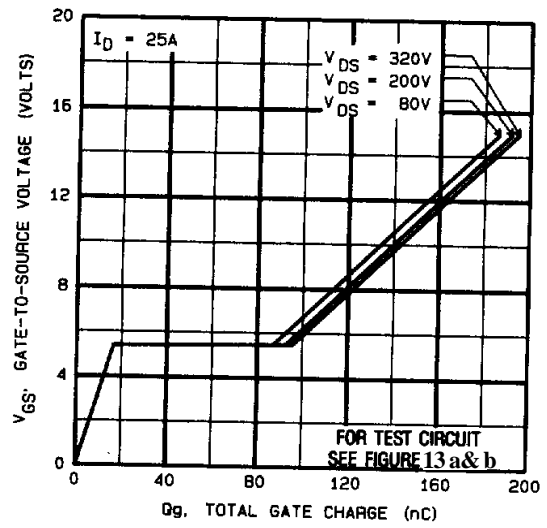


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

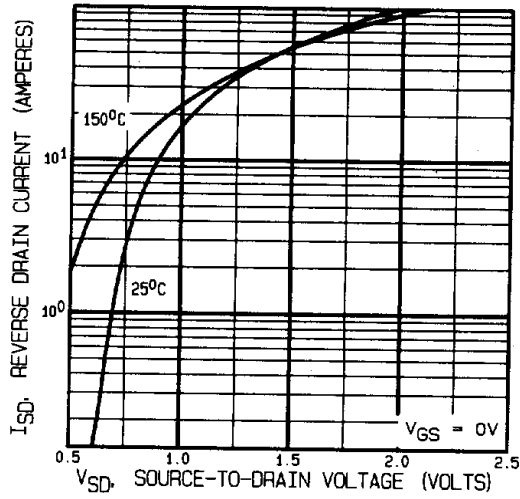


Fig 7. Typical Source-Drain Diode Forward Voltage

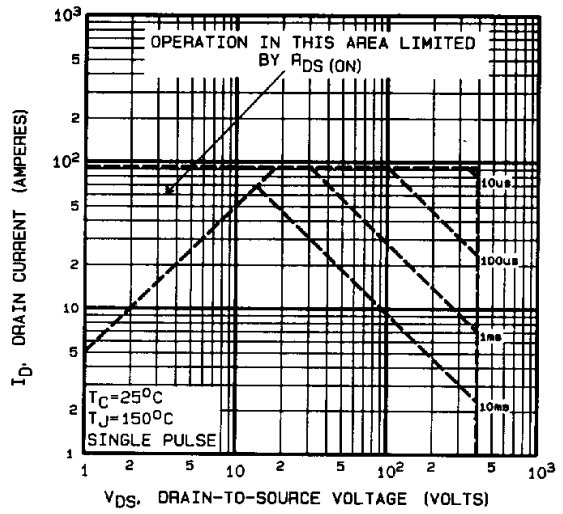


Fig 8. Maximum Safe Operating Area

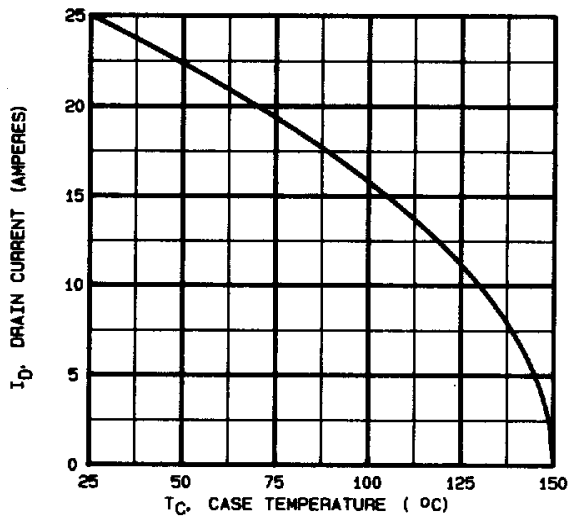


Fig 9. Maximum Drain Current Vs. Case Temperature

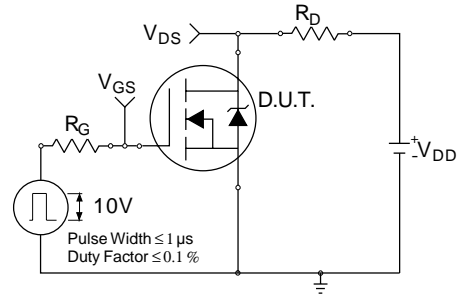


Fig 10a. Switching Time Test Circuit

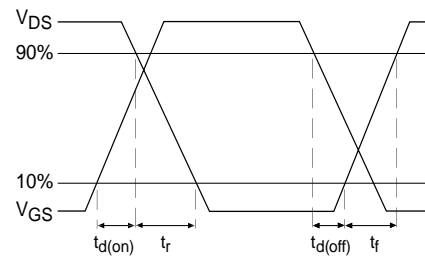


Fig 10b. Switching Time Waveforms

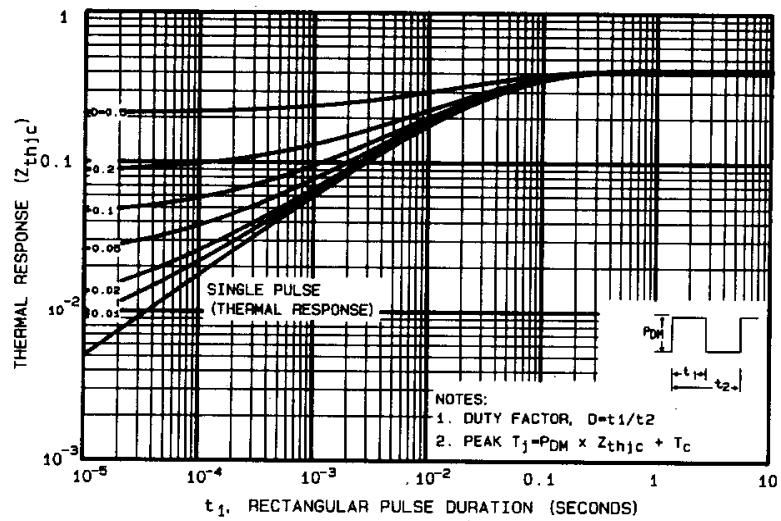


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

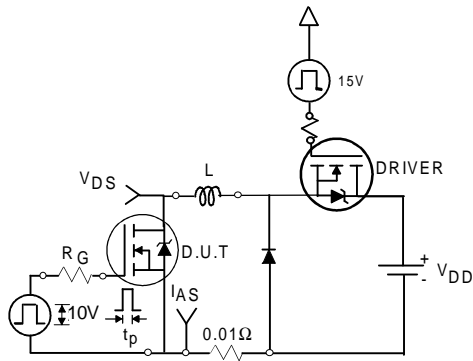


Fig 12a. Unclamped Inductive Test Circuit

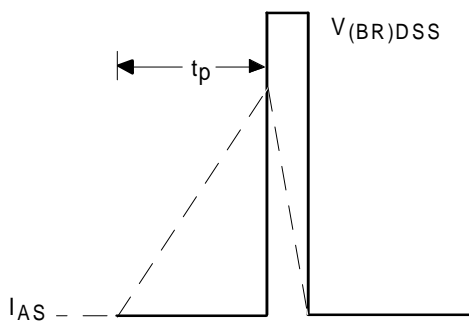


Fig 12b. Unclamped Inductive Waveforms

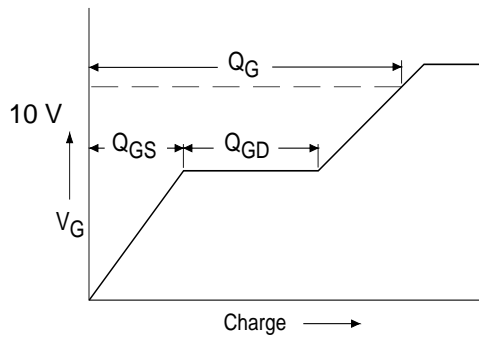


Fig 13a. Basic Gate Charge Waveform

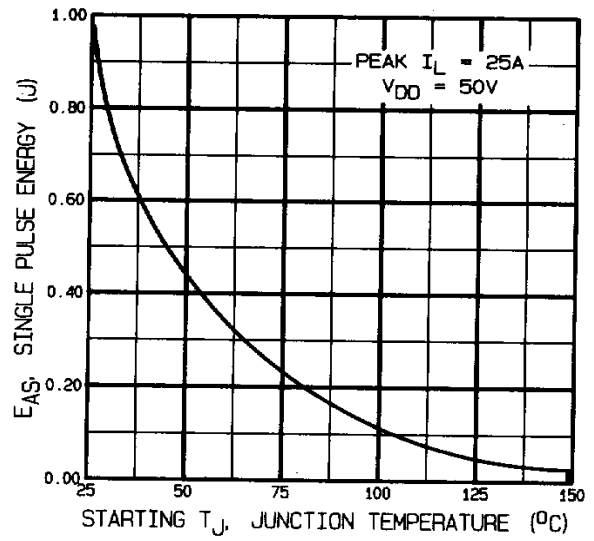


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

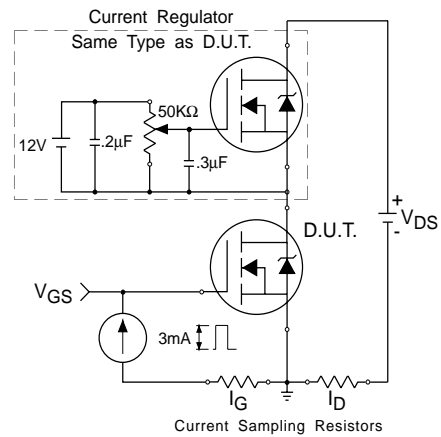


Fig 13b. Gate Charge Test Circuit