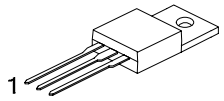
YAREN TECHNOLOGY

YR1404

Power MOSFET

190 Amps 40 Volts
N-CHANNEL POWER MOSFET



TO-220

*Pb-free plating product number: YR1404

■ DESCRIPTION

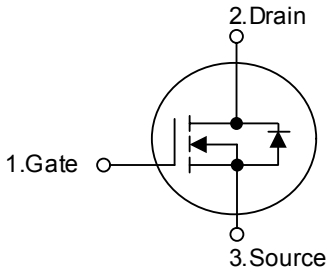
The YR 1404 is three-terminal silicon device with current conduction capability of about190A, fast switching speed. Low on-state resistance, breakdown voltage rating of 40V, and max threshold voltages of 4 volt.

It is mainly suitable electronic ballast, and low power switching mode power appliances.

■ FEATURES

* $R_{DS(ON)}$ = 3.7mΩ@V_{GS} = 10 V
* Ultra low gate charge (typical 163 nC)
* Low reverse transfer Capacitance (C_{RSS} = typical 780 pF)
* Fast switching capability
* 100% avalanche energy specified
* Improved dv/dt capability

■ SYMBOL



Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	190	A
I_D @ T_C = 100°C	Continuous Drain Current, VGS @ 10V (Silicon Limited)	134	
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Package Limited)	170	
I_{DM}	Pulsed Drain Current ①	750	
P_D @T_C = 25°C	Power Dissipation	220	W
	Linear Derating Factor	1.47	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy (Thermally Limited)	1200	mJ
E_{AS} (tested)	Single Pulse Avalanche Energy Tested Value	1400	
I_{AR}	Avalanche Current	See Fig.12a, 12b, 15, 16	A
E_{AR}	Repetitive Avalanche Energy		mJ
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	0.68	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat Greased Surface	0.50	——	
$R_{\theta JA}$	Junction-to-Ambient	——	62	
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount)	——	40	

Static Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	——	——	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.033	——	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	2.7	3.7	mΩ	V_{GS} = 10V, I_D = 40A
$V_{GS(th)}$	Gate Threshold Voltage	2.0	——	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
gfs	Forward Transconductance	170	——	——	V	V_{DS} = 50V, I_D = 75A
I_{DSS}	Drain-to-Source Leakage Current	——	——	1	μA	V_{DS} = 40V, V_{GS} = 0V
		——	——	100		V_{DS} = 40V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	——	——	-100		V_{GS} = -20V

Dynamic Electrical @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge	——	163		nC	I_D = 30A
Q_{gs}	Gate-to-Source Charge	——	31	——		V_{DS} = 30V
Q_{gd}	Gate-to-Drain ("Miller") Charge	——	64	——		V_{GS} = 10V
$t_{d(on)}$	Turn-On Delay	——	26	——	nS	V_{DD} = 30V
t_r	Rise Time	——	24	——		I_D = 2A
$t_{d(off)}$	Turn-Off Delay	——	91	——		R_G = 2.5 Ω
t_f	Fall Time	——	58	——		V_{GS} = 10V
L_D	Internal Drain Inductance	——	4.5	——	nH	Between lead, 6mm (0.25in.)
L_S	Internal Source Inductance	——	7.5	——		from package and center of die contact
C_{iss}	Input Capacitance	——	6500	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	916	——		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	——	780	——		f = 1.0MHz
C_{oss}	Output Capacitance	——	5500	——		V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz
C_{oss}	Output Capacitance	——	830	——		V_{GS} = 0V, V_{DS} = 32V, f = 1.0MHz
C_{oss} eff.	Effective Output Capacitance	——	650	——		V_{GS} = 0V, V_{DS} = 0V to 32V ④

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	190	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode)	—	—	850		
V_{SD}	Diode Forward Voltage	—	—	1.2	V	T_J = 25°C, I_S = 40A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	—	42	60	ns	T_J = 25°C, I_F = 40A, V_{DD} = 20V
Q_{rr}	Reverse Recovery Charge	—	66	80	nC	di/dt = 100A/μs
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

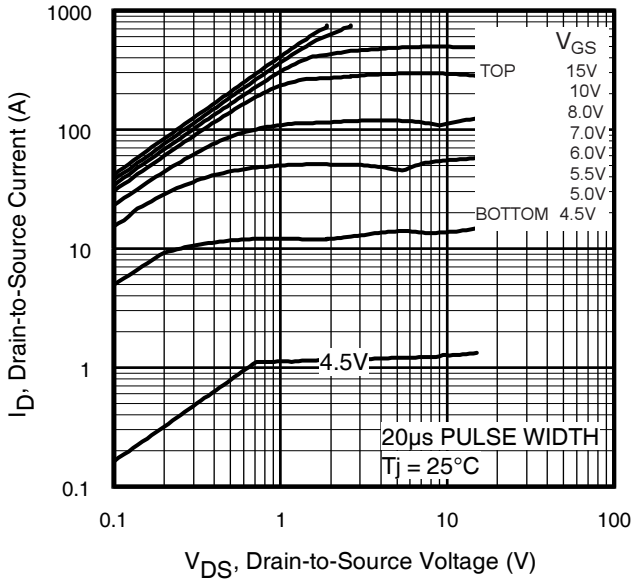


Fig 1. Typical Output Characteristics

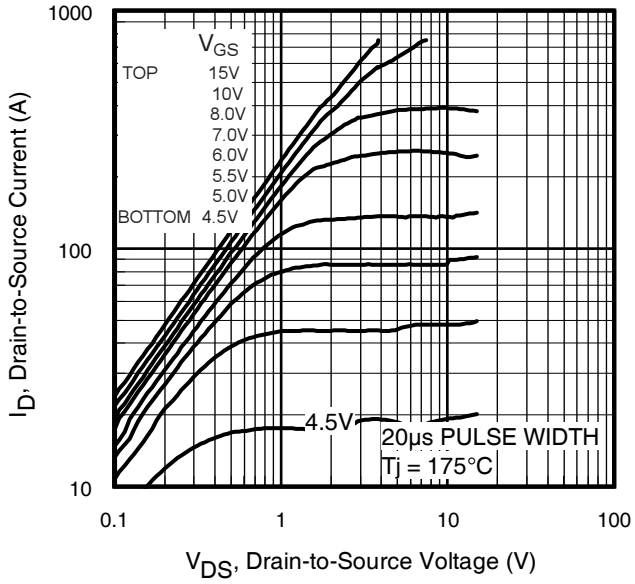


Fig 2. Typical Output Characteristics

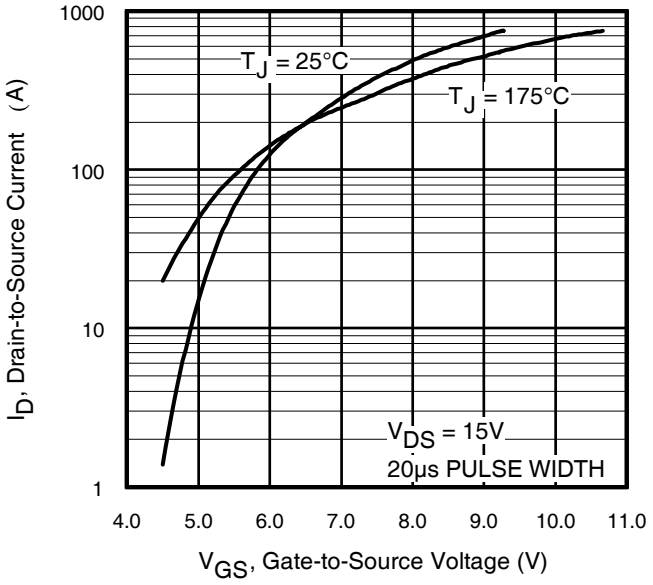


Fig 3. Typical Transfer Characteristics

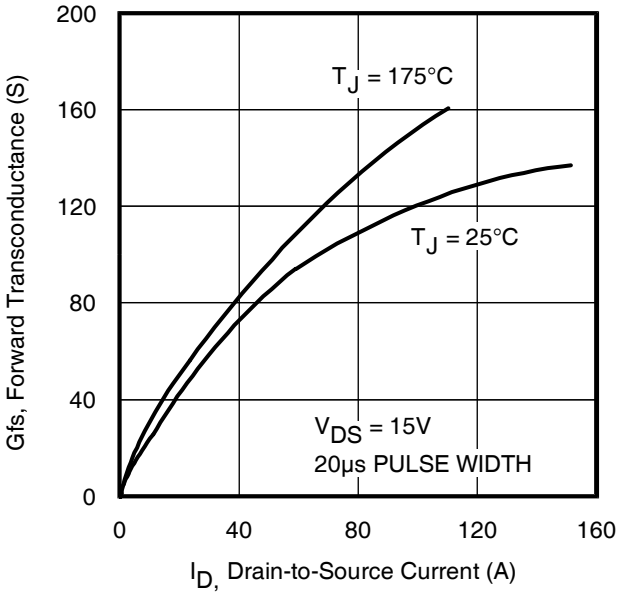


Fig 4. Typical Forward Transconductance Vs. Drain Current

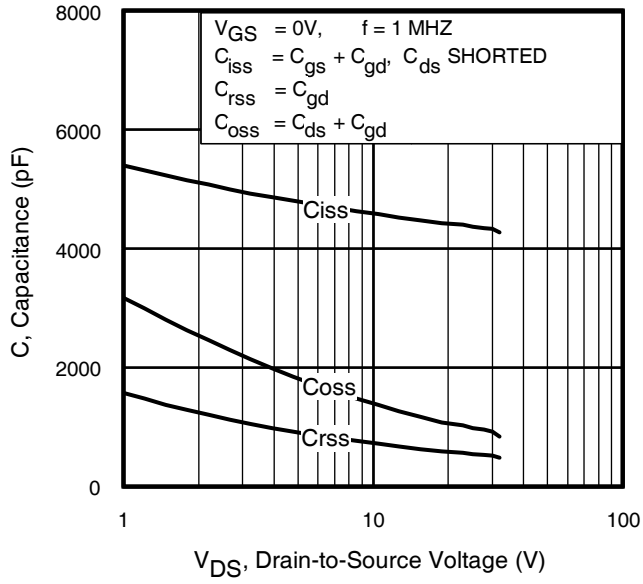


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

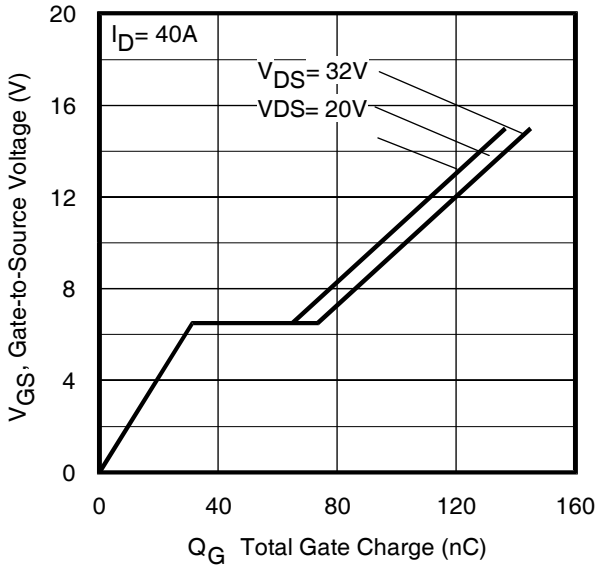


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

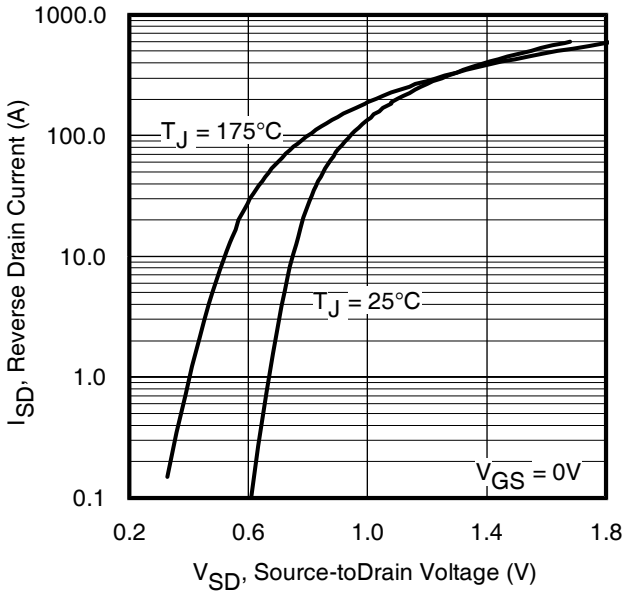


Fig 7. Typical Source-Drain Diode Forward Voltage

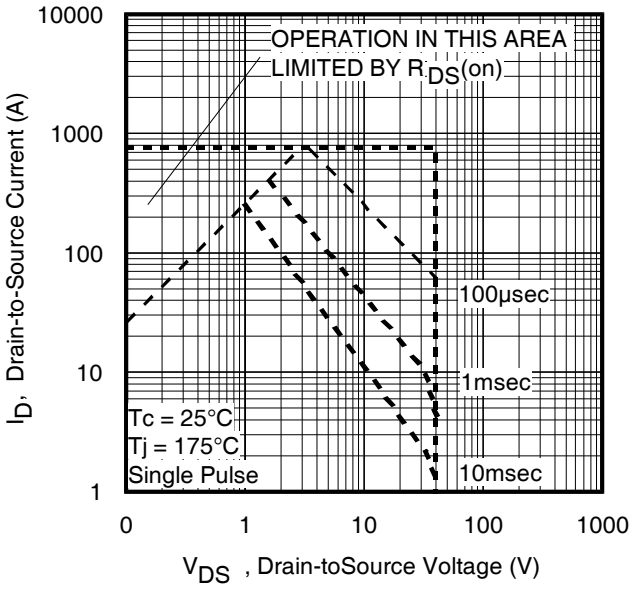


Fig 8. Maximum Safe Operating Area

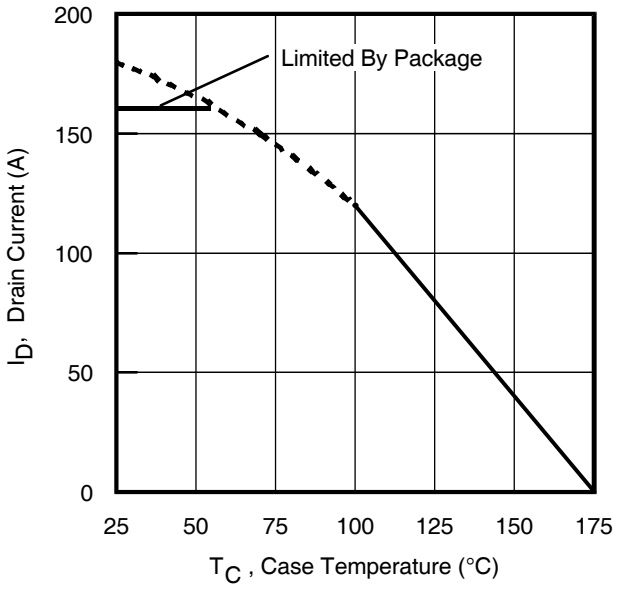


Fig 9. Maximum Drain Current Vs. Case Temperature

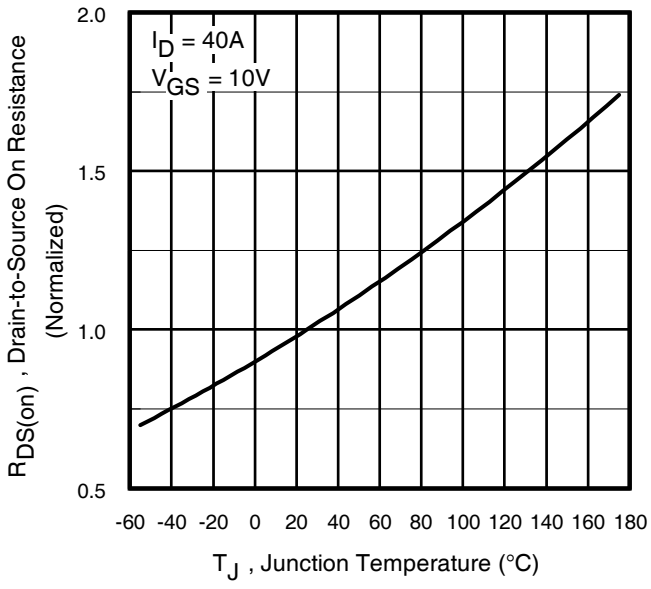


Fig 10. Normalized On-Resistance Vs. Temperature

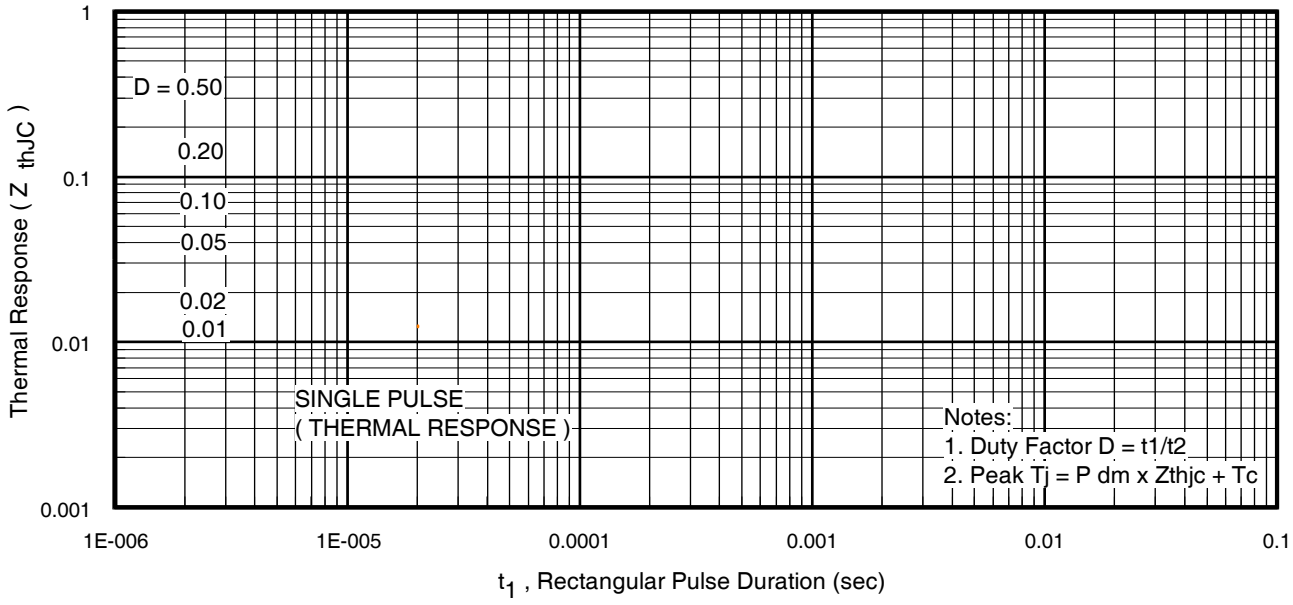


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

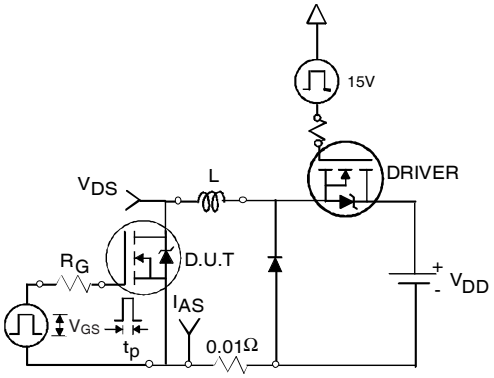


Fig 12a. Unclamped Inductive Test Circuit

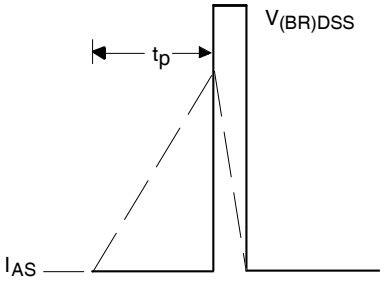


Fig 12b. Unclamped Inductive Waveforms

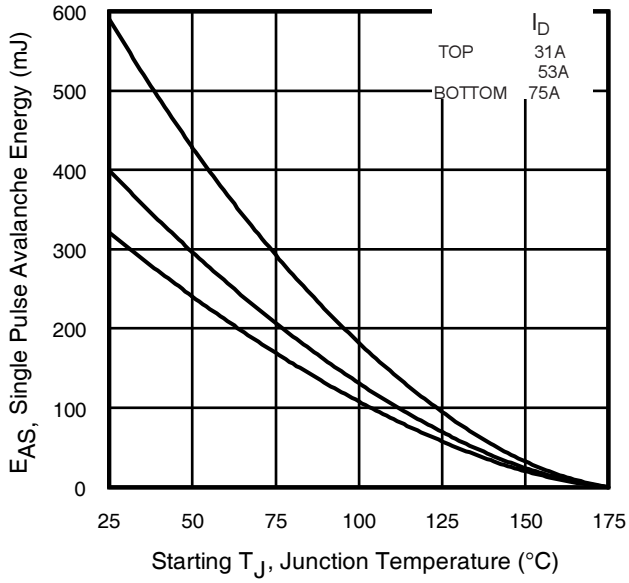


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

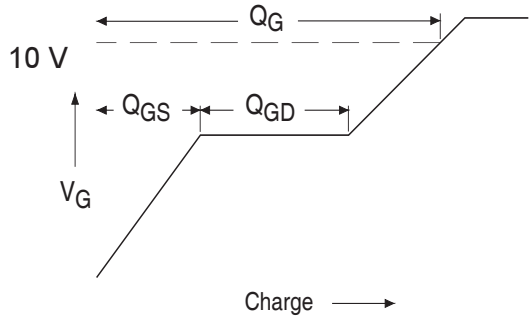


Fig 13a. Basic Gate Charge Waveform

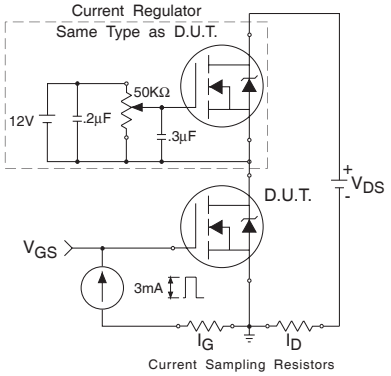


Fig 13b. Gate Charge Test Circuit

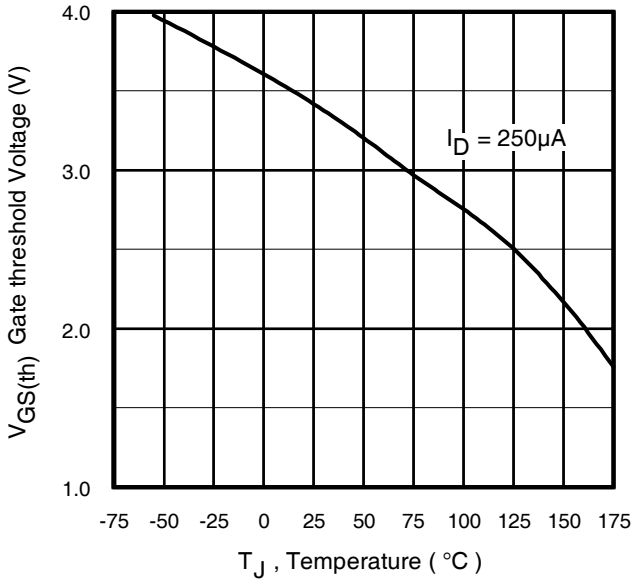


Fig 14. Threshold Voltage Vs. Temperature

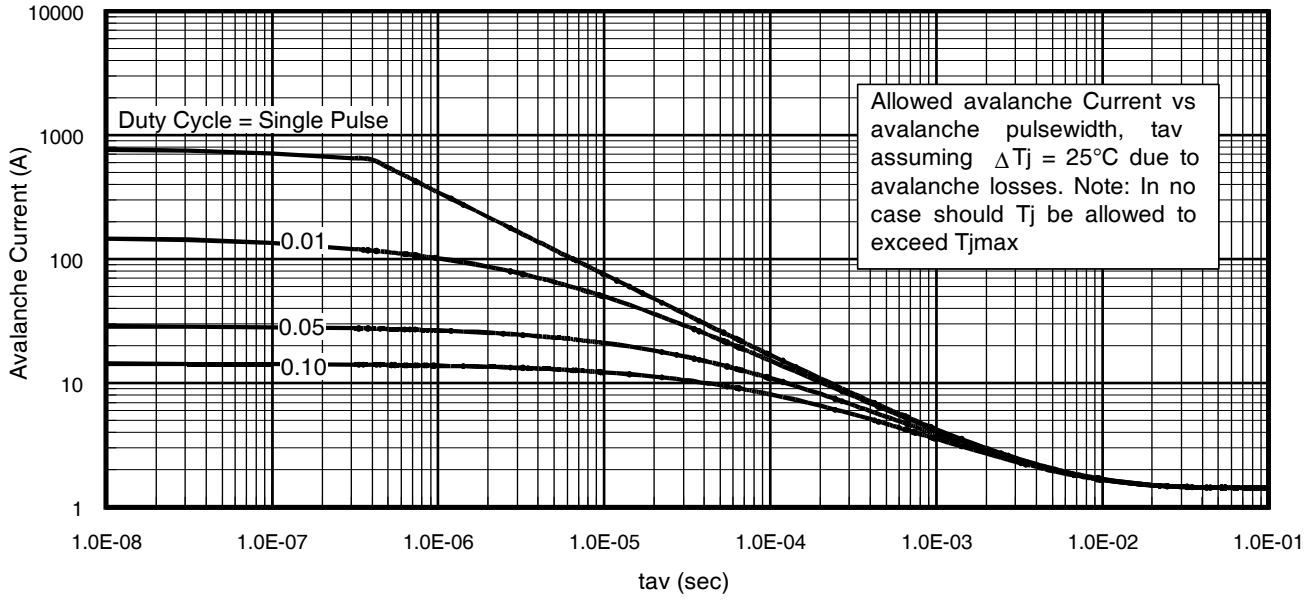


Fig 15. Typical Avalanche Current Vs.Pulsewidth

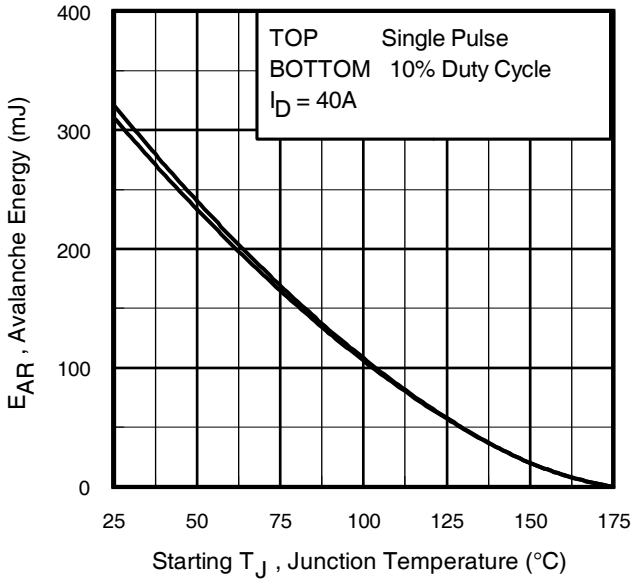


Fig 16. Maximum Avalanche Energy Vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16: (For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption: Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long asT_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$P_{D\ (ave)} = 1/2\ (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$

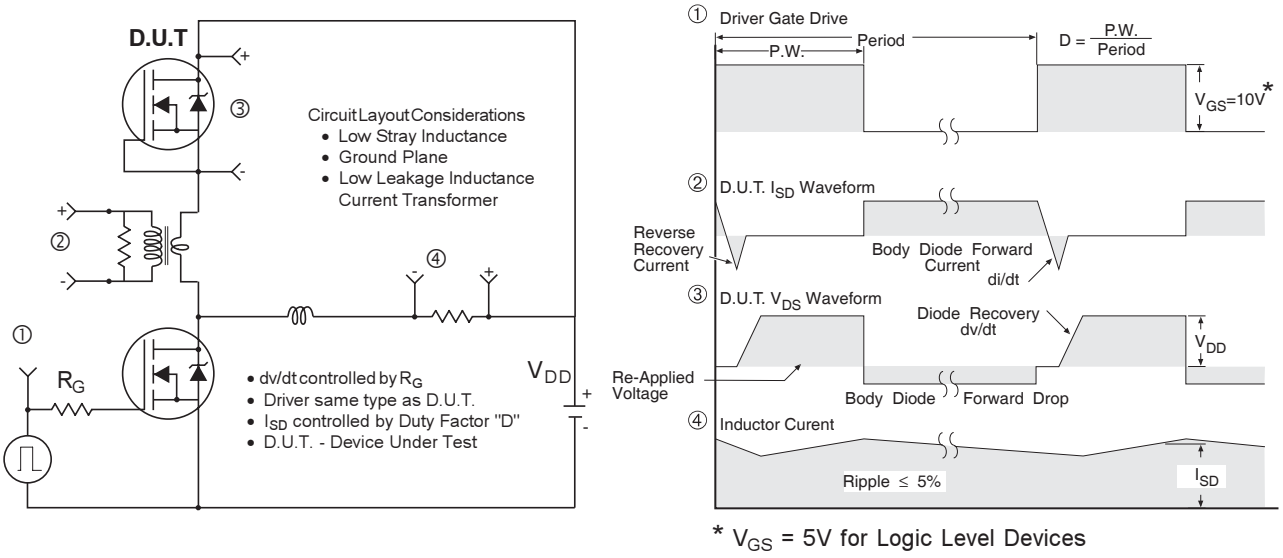


Fig 17. Peak Diode Recovery dv/dt Test Circuit for N-Channel

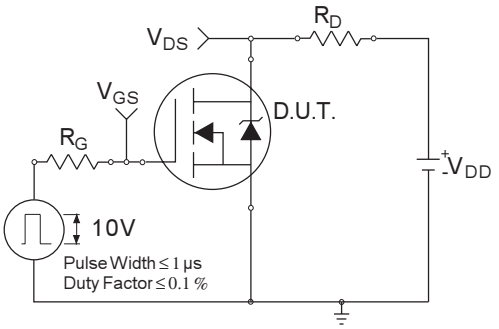


Fig 18a. Switching Time Test Circuit

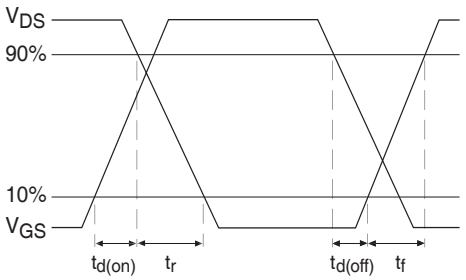


Fig 18b. Switching Time Waveforms